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| NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION | | | CHIO, TAT CHI | |
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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| Office Action Summary | Application No. 10/064,352 | Applicant(s) CHEN, KUAN-CHOU | |
| | Examiner Tat Chi Chio | Art Unit 2621 | |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on Amendment filed on 18 July 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-9 and 12-17 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-9 and 12-17 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 7/18/2007 have been fully considered but they are not persuasive.
2. In response to Applicant's argument "a combined teaching of Cho and Romano fails to teach or suggest the claimed feature "the decoder circuit, the graphics decoding circuit and the memory controller are either fabricated on a monolithic substrate or within a packaging substrate", Cho discloses the decoder circuit (200 of Fig. 1, ECC 116 is shown in Fig. 2, which is the detailed view of system decoder of Fig. 1), the graphics decoding circuit (A/V decoder 600 of Fig. 1) and the memory controller (1st memory controller 121 and 2nd memory controller 122 of Fig. 2), and Romano et al. teach "a single monolithic integrated circuit ("IC") embodying all or substantially all of the motion control and processing functionality of a disk drive" (col. 3, lines 2-5).
3. In response to Applicant's argument "the memory controller and external memory of Claim 1 are neither taught nor suggested by the combined result indicated by the examiner", Cho discloses an external memory in Fig. 1 (memory 280 of Fig. 1) and the memory controller in Fig. 2 (1st memory controller 121 and 2nd memory controller 122 of Fig. 2).
4. In response to Applicant's argument "Cho's disclosure fails to teach or suggest allowing both the system decoder and the A/V decoder to write data into a shared external memory", Cho shows in Fig. 1 the arrow between the external memory 280 and the system decoder is two-way direction and a second memory controller connected to

the second data bus 127 controls the data writer 118, the microcomputer memory access controller 119, and the A/V decoder interface and DVD-ROM interface 120 makes access to the second memory (col. 2, lines 44-51).

5. In response to Applicant's argument "By utilizing a single memory controller, the system disclosed in Claim 1 overcomes the need for two separate RAM banks and reduces complexity and cost of production. As the use of the single memory controller is not simply an engineering choice but yields benefits not anticipated by the teachings of the prior art", since making two memory controllers into one minimizes the space, size, and weight of the device and this minimization is a common in engineering. Therefore, it is obvious to one of ordinary skill in the art at the time the invention was made to make two memory controllers into a single memory controller.

Claim Rejections - 35 USC § 103

1. Claims 1-4, 6-8, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cho (US 6,859,614 B1) in view of Romano et al. (5,586,306).

Consider claims 1 and 12, Cho discloses an electronic circuit comprising:

- a servo control (disk drive controller 400 of Fig. 1) and ECC decoder circuit (system decoder 200 of Fig. 1. ECC 116 is shown in Fig. 2 that is the detailed view of system decoder of Fig. 1) for controlling a removable media device to obtain encoded data from a removable media, and for performing a decoding process to obtain decoded data from the encoded

data and storing the decoded data in an external memory (memory 280 of Fig. 1);

- a graphics decoding circuit (A/V decoder 600 of Fig. 1) for decoding graphics data held in the external memory to generate video data and audio data; and
- a memory controller to provide read and write access to the external memory for both the servo control and ECC decoder circuit and the graphics decoding circuit (1st memory controller 121 and 2nd memory controller 122 of Fig. 2);
- wherein the graphics decoding circuit performs a graphics decoding process on the decoded data to generate the video data and audio data (col. 1, lines 65-67 and col. 2, lines 1-3).

Cho discloses two memory controllers instead of one memory controller as in the application. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine two memory controllers into one memory controller since it has been held "that the use of one piece construction instead of the structure disclosed in [the prior art] would be merely a matter of obvious engineering choice." *In re Larson*, 340 F.2d 965, 968, 144 USPQ 347, 349 (CCPA 1965).

Cho discloses all the limitations above but fails to disclose the decoder circuit, the graphics decoding circuit, and the memory controller are either fabricated on a monolithic substrate or within a packaging substrate

Romano et al. teaches the decoder circuit, the graphics decoding circuit, and the memory controller are either fabricated on a monolithic substrate or within a packaging substrate (col. 3, lines 1-4, col. 6, lines 60-51 and 65-66). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to fabricate the removable media device driver and decoder circuit, the graphics decoding circuit and the memory controller on the monolithic substrate since monolithic integration provides advantages include: smaller size, greater functionality, lower power requirement, improved reliability, tighter manufacturing tolerances, and simplified packaging.

Consider claim 2, Cho discloses the electronic circuit, wherein the graphics decoding circuit utilizes the memory controller to store the video data in the external memory (col. 2, lines 44-50).

Consider claim 3, Cho discloses the electronic circuit further comprising video output circuitry for generating a video signal for an external display device according to the video data (col. 1, lines 66-67 and col. 2, lines 1-3).

Consider claim 4, Cho discloses the electronic circuit further comprising a communications pathway electrically linking the Servo control and ECC decoder circuit with the graphics decoding circuit to permit the servo control and ECC decoder circuit and the graphics decoding circuit to exchange information (Fig. 1).

Consider claim 6, Cho discloses the electronic circuit wherein the servo control and ECC decoder circuit comprises a signal to indicate to the graphics decoding circuit that newly decoded data is available in the external memory (col. 6, lines 15-20).

Consider claim 7, Cho discloses the electronic circuit wherein the servo control and ECC decoder circuit is adapted to decode data received from a digital video disk (DVD) removable media, or a compact disk (CD) removable media (col. 4, lines 63-65).

Consider claim 8, Cho discloses the electronic circuit wherein the servo control and ECC decoder circuit is adapted to control a DVD-type drive, or a CD-type drive (col. 4, lines 31-35).

2. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cho (US 6,859,614 B1) in view of Romano et al. (5,586,306) as applied to claims 1-4, 6-8, and 12 above, and further in view of Chau (5,870,087).

Consider claim 9, Cho discloses all the limitations in claim 1, but fails to explicitly disclose the electronic circuit wherein the graphics decoding circuit performs a Moving Picture Experts Group (MPEG) type graphics decoding process to generate the video data. Chau teaches the electronic circuit of wherein the graphics decoding circuit performs a Moving Picture Experts Group (MPEG) type graphics decoding process to generate the video data (col. 6, lines 51-52). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate a MPEG decoder in the electronic circuit to generate the video data since

the MPEG compression technique is more efficient than other video and audio compression technique.

3. Claims 5, 13, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cho (US 6,859,614 B1) in view of Romano et al. (5,586,306) as applied to claims 1-4, 6-8, and 12 above, and further in view of Yuen et al. (US 2003/0190138 A1).

Consider claim 5, Cho discloses all the limitations in claim 1, but fails to disclose the electronic circuit wherein the servo control and ECC decoder circuit further comprises a register accessible by the graphics decoding circuit that indicates the location of decoded data in the external memory.

Yuen et al. teach the electronic circuit wherein the servo control and ECC decoder circuit further comprises a register accessible by the graphics decoding circuit that indicates the location of decoded data in the external memory (directory controller of Fig. 5). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate a directory controller to indicate the location of the video program since the program directory will eliminate much of the frustration that has been felt for so long by so many users of tape devices ([0022]).

Consider claim 13, Yuen et al. further discloses the electronic circuit, wherein the servo control and ECC decoder circuit further comprises: a first register indicating a first storage location in the external memory for the encoded data from the removable media; a second register indicating a second storage location in the external memory

for the decoded data which is decoded from the encoded data; and a third register indicating a size of the decoded data (directory controller of Fig. 5).

Consider claim 14, Yuen et al. further discloses the electronic circuit, wherein the second storage location overlaps the first storage location ([0875], since the controller adjusts the length due to overlap of programs, the programs overlap each other.)

4. Claims 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cho (US 6,859,614 B1) in view of Romano et al. (5,586,306) as applied to claims 1-4, 6-8, and 12 above, and further in view of Iwamura (5,838,876).

Consider claim 15, Cho and Romano et al. disclose all the limitations in claim 12, but fail to disclose the electronic circuit, wherein the graphics decoder circuit further comprises: a video head pointer indicating a first address where a newest video data is stored in the external memory; an audio head pointer indicating a second address where a newest audio data is stored in the external memory; a video tail pointer indicating a third address where an oldest video data is stored in the external memory; an audio tail pointer indicating a fourth address where an oldest audio data is stored in the external memory, wherein the video head pointer and the video tail pointer constitute a video circular buffer in the external memory, and the audio head pointer and the audio tail pointer constitute an audio circular buffer in the external memory.

Iwamura teaches the electronic circuit, wherein the graphics decoder circuit further comprises: a video head pointer indicating a first address where a newest video data is stored in the external memory; an audio head pointer indicating a second address where a newest audio data is stored in the external memory; a video tail pointer indicating a third address where an oldest video data is stored in the external memory; an audio tail pointer indicating a fourth address where an oldest audio data is stored in the external memory, wherein the video head pointer and the video tail pointer constitute a video circular buffer in the external memory, and the audio head pointer and the audio tail pointer constitute an audio circular buffer in the external memory (col. 5, lines 29-50). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate a ring buffer in the external memory since the ring buffer provides fast and efficient access to data.

Consider claim 16, Iwamura further teaches the electronic circuit, wherein the graphics decoder circuit stops the graphics decoding process when either the video head pointer is about to write over the video tail pointer or the audio head pointer is about to write over the audio tail pointer, so as to prevent loss of the video data or the audio data respectively (col. 5, lines 55-56).

Consider claim 17, Iwamura further teaches the electronic circuit, wherein the graphics decoder circuit resumes the video tail pointer when the video tail pointer advances close enough to the video head pointer, or resumes the audio tail pointer when the audio tail pointer advances close enough to the audio head pointer (col. 6, lines 7-9).

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tat Chi Chio whose telephone number is (571) 272-9563. The examiner can normally be reached on Monday - Thursday 8:30 AM-6:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thai Tran can be reached on (571)-272-7382. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2621

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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